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Subject: genius needed

Posted by [jeremy luzier\[1\]](#) on Mon, 28 Jul 2008 16:07:04 GMT

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>

>Well, an hour of testing and it seems solid here, both with PARIS and through ASIO. I can't tell the difference from the last build, but I guess that's the point.

If you're tackling the IRQ assignment glitches in the PSCL, and everything depends upon the PSCL - do you think this could also have a global positive effect on PARIS' IRQ twitchiness overall?

- K

On 2008-09-21 10:03:35 -0700, "Mike Audet" <mike@...> said:

>

> Thanks, Kerry!

>

> In the latest build, I reset the delays to zero. So, it should be faster.

>

> Cheers!

>

> MikeHi Kerry,

I've just been looking at the Scherzo and I'm certain I know what has been happening. There is function that is called when the hardware interrupts called an ISR. It does the following:

- 1) read what the interrupt state is.
- 2) set the interrupt state to mas